Appl. No. 10/520,866
APPEAL BRIEF

IN THE UNITED STATES

PATENT AND TRADEMARK OFFICE

Appl. No: 10/520,866

Applicant(s): Guillaume De Cremoaux, et al.

Filed: January 11, 2005

Title: Capacitive Feedback Circuit

T.C./A.U.: 2800/2838

Examiner: Shawn Riley

Atty. Docket No. NL020624

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On: 14 August 2007

By: Judith Riddell

APPEAL BRIEF

Honorable Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In connection with the Notice of Appeal dated June 14, 2007, Applicants provide the following Appeal Brief in the above captioned application.

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TABLE OF CASES

1. W.L. Gore & Associates, Inc. v. Garlock, Inc., 220 USPQ 303 (CAFC 1983).
2. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994)
3. In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990).
4. Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992).
5. Scripps Clinic & Res. Found. v. Genentech, Inc., 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

1. Real Party in Interest

As a result of a divestiture of assets Koninklijke Philips N.V. to NXP Semiconductors, and the ownership of certain patent applications were transferred. The undersigned attorney is acting on the good-faith belief that the present application is part of that transfer. As such, the present Appeal Brief is being filed on behalf of NXP Semiconductors, having a principle place of business at High Tech Campus 60, P.O.Box 80073, 5600 KA Eindhoven, The Netherlands.

2. Related Appeals and Interferences

There are no known related appeals or interferences at this time.

3. Status of the Claims

Claims 1-17 are pending in the present application. Claims 1-12, 15-16 have been finally rejected. Claims 13,14 and 17 are objected to. The claims 1-17 are duplicated in the Appendix.

4. Status of Amendments

A Final Office Action on the merits was mailed on March 14, 2007. A Notice of Appeal was filed on June 14, 2007; and a Response under Rule 116 was filed to address some issues with the Drawings on June 21, 2007. An Advisory Action dated July 17 was received.

5. Summary of the Claimed Subject Matter[1]

In one embodiment, a capacitive feedback circuit (20) comprises a voltage input terminal (21) a current output terminal (22). The circuit (20) also includes a feedback

1 In the description to follow, citations to various reference numerals, drawings and corresponding text in the specification are provided solely to comply with Patent Office Rules. It is emphasized that these reference numerals, drawings and text are representative in nature, and in not any way limiting of the true scope of the claims. It would therefore be improper to import any meaning into any of the claims simply on the

capacitor (23), having a first terminal connected to the input terminal (21) and having a second terminal connected to a high-impedance node (N). (Kindly refer to claim 1; page 4, lines 24-33; and Fig 2.)

6. Grounds of Rejection to be Reviewed on Appeal

The issues in the present matter are whether:

I. Any basis of rejection has been made as to claim 15; and

II. Claims 1-12 and 16 are properly rejected under 35 U.S.C. § 102(e) in view of *Yakabe* (US Patent 7,088,112).

7. Argument

In this portion of the Appeal Brief, arguments are provided. Notably, because no claims have been amended or allowed, Applicants maintain previous arguments for patentability provided in response to Office Actions.

I. Claim 15 is patentable

At the outset Applicants note that the Office Action fails to provide any substantive basis for the rejection of claim 15. Because a *prima facie* case rejecting this claim under any of the applicable U.S. patent laws has not been even been offered, let alone established, Applicants respectfully submit that this claim should be indicated as allowable.

basis of illustrative language that is provided here only under obligation to satisfy Patent Office rules for maintaining an Appea

II. Claims 1-12 and 16 are patentable over the applied art

Applicants rely at least on the following standards with regard to proper rejections under 35 U.S.C. § 102. Notably, a proper rejection of a claim under 35 U.S.C. § 102 requires that a single prior art reference disclose each element of the claim. *See, e.g., W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983). Anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. *See, e.g., In re Paulsen,* 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Alternatively, anticipation requires that each and every element of the claimed invention be embodied in a single prior art device or practice. *See, e.g., Minnesota Min. & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 18 USPQ2d 1001 (Fed. Cir. 1991).

i. Rejection under 35 U.S.C. § 102(e) of claims 1-12 in view of *Yakabe*

Claim 1 is drawn to a capacitive feedback circuit. The circuit comprises, among other features, a feedback capacitor, having a first terminal connected to the input terminal and having a second terminal connected to a high-impedance node.

a. Yakabe fails to disclose a feedback capacitor as claimed

In a representative embodiment described in the filed application in connection with Fig. 2, a capacitive feedback circuit 20 includes a feedback capacitor 23, having a first

terminal connected to input terminal 21 and a second terminal connected to a high-impedance node. (Kindly refer to page 4, lines 24-29 of the filed application.)

The Office Action asserts that the reference to *Yakabe* discloses the noted features of claim 1. To wit, the Office Action asserts that in the description of Fig. 4 *Yakabe* discloses a voltage input terminal (Vin) and a feedback capacitor (C), having a first terminal connected to the input terminal

The reference to *Yakabe* fails to disclose that the capacitor (C) is a feedback capacitor, or that one of its terminals in connected to the input terminal. Rather, the reference discloses that at a first terminal, the first capacitor (C) connects to an output of an operational amplifier (OP1) and the **output voltage (Vout) terminal (OUT)** of the circuit. Thus, the capacitor (C) of *Yakabe* does not have a terminal connected to the **voltage input terminal** ((Vin) according to the position of the Office Action), but rather to an output terminal (Vout, OUT). Moreover, there is no mention of the capacitor's being a feedback capacitor, nor is the circuit configured as such.

In the Final Office Action, the Examiner states:

C is a feedback capacitor since the input (Vin) is feedback to the C via R1/R2/R3.

It is unclear how the input voltage is feedback to the capacitor C, or how this renders the capacitor C of Fig. 4 of the applied art a feedback capacitor. Moreover, no citation has been provided in the applied art of the assertion reproduced above. Thus, a clearly articulated rejection in compliance with MPEP § 706 has not been provided.

For at least the reasons set forth above, Applicant respectfully submits that the reference to *Yakabe* fails to disclose at least one feature of independent claim 1, and that there is at least one difference between claim 1 and the applied art as viewed by a person of ordinary skill in the art. Therefore, a prima facie case of anticipation has not been made and claim 1 and the claims that depend therefrom are patentable over *Yakabe*.

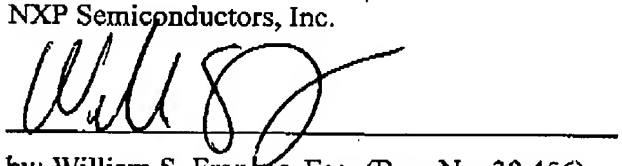
For at least the reasons set forth above, it is respectfully submitted that the rejection of claims 1 and is improper and should be withdrawn. Moreover, by similar reasoning, it is respectfully submitted that the rejection of claims 2-12, and 16, which depend immediately or ultimately from claim 1 are also improper and should be withdrawn.

8. Conclusion

In view of the foregoing, applicant(s) respectfully request(s): the withdrawal of all objections and rejections of record; the allowance of all the pending claims; and the holding of the application in condition for allowance.

Respectfully submitted on behalf of:

NXP Semiconductors, Inc.



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Appendix

Claims on Appeal

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Claims on Appeal:

1. Capacitive feedback circuit, comprising: a voltage input terminal; a current output terminal; a feedback capacitor, having a first terminal connected to the input terminal and having a second terminal connected to a high-impedance node.

2. Capacitive feedback circuit according to claim 1, further comprising: an amplifying element having a high-impedance control terminal connected to said node; a current sensor connected in series between said amplifying element and a first supply voltage; a bias current source connected in series between said amplifying element and a second supply voltage.

3. Capacitive feedback circuit according to claim 2, wherein said current sensor is part of a current-to-voltage converting feedback loop, which has a high-impedance output terminal connected to said node.

4. Capacitive feedback circuit according to claim 3, wherein the current sensor has an output providing a current output signal, and wherein the feedback loop comprises a comparator, having one current input connected to said current output of the current sensor, having a second input connected to receive a reference current, and having a voltage output connected to said node.

5. (Previously Presented) Capacitive feedback circuit according to claim 2, wherein the output terminal is connected to the node between the amplifying element and the bias current source.

6. (Previously Presented) Capacitive feedback circuit according to claim 2, wherein the output terminal is connected to the node between the amplifying element and the current sensor.

7. (Previously Presented) Capacitive feedback circuit according to claim 2, wherein the amplifying element comprises a first transistor, preferably a MOSFET, having its gate connected to said node.

8. (Previously Presented) Capacitive feedback circuit according to claim 2, wherein the bias current source comprises a second transistor, preferably a MOSFET, having its source connected to second supply voltage, and having its gate connected to a source of accurate constant bias voltage.

9. (Previously Presented) Capacitive feedback circuit according to claim 7, wherein the second transistor has its drain connected to the source of the first transistor.

10. (Previously Presented) Capacitive feedback circuit according to claim 2, wherein the current sensor comprises a combination of two transistors, preferably MOSFETs, connected in a current mirror configuration.

11. (Previously Presented) Capacitive feedback circuit according to claim 7, wherein the current sensor comprises a third transistor having its source connected to first supply voltage and having its drain connected to the drain of the first transistor, and further comprises a fourth transistor having its source connected to first supply voltage and having its gate connected to the gate and to the drain of the third transistor.

12. (Previously Presented) Capacitive feedback circuit according to claim 2, wherein the comparator comprises a combination of two transistors, preferably MOSFETs, connected in a current mirror configuration.

13. Capacitive feedback circuit according to claim 11, wherein the comparator comprises a fifth transistor having its source connected to second supply voltage and having its drain connected to the drain of the fourth transistor, and further comprises a sixth transistor having its source connected to second supply voltage and having its gate connected to the gate and to the drain of the fifth transistor.

14. Capacitive feedback circuit according to claim 13, wherein the comparator further comprises a reference current source coupled to provide a reference current to the drain of the sixth transistor, and wherein the drain of the sixth transistor is connected to said node.

15. Capacitive feedback circuit according to claim 14, wherein the reference current source a seventh transistor having its source connected to first supply voltage, having its drain connected to the drain of the sixth transistor, and having its gate connected to a source of accurate constant reference voltage.

16. (Previously Presented) Voltage regulator comprising a capacitive feedback circuit according to claim 1.

17. Voltage regulator comprising: a voltage input terminal; a voltage output terminal; an input differential amplifier, comprising a differential input stage which comprises: a first series arrangement of a first transistor, preferably a MOSFET, and a first current source; a second series arrangement of a second transistor, preferably a MOSFET, and a second current source; and a non-linear resistor having a first terminal connected to a first node between the first transistor and the first current source and having a second terminal connected to a second node between the second transistor and the second current source; said input differential

amplifier having a signal input terminal connected to the regulator input terminal; an output driver stage comprising: a voltage input connected to an output of the input differential amplifier; a voltage output; a current feedback loop feeding back a signal representative of the output current provided at said voltage output such as to effectively decrease the AC-impedance at said voltage input in order to increase the gain for AC signals; voltage feedback means having an input connected to the regulator output terminal and having an output connected to a feedback input terminal of the input stage; and a capacitive feedback circuit according to claim 1, having its input terminal connected to the regulator output terminal and having its output terminal connected to the input of the output driver stage; wherein said voltage regulator further has one or more of the following features: (a) the non-linear resistor comprises a third transistor, preferably a MOSFET, having its source connected said first node, having its drain connected to said second node, and having its gate connected to a constant bias voltage; (b) the first current source is connected between a source of the first transistor and a voltage reference; the second current source is connected between a source of the second transistor and said voltage reference; and said three transistors mutually are of the same conductivity type; (c) the output driver stage comprises: an input transistor, preferably a MOSFET, having its source connected to a controllable impedance, and having its gate connected to the input terminal; wherein said controllable impedance preferably comprises: two transistors, preferably MOSFETS, connected in current mirror configuration, wherein a first one of said transistors has its source connected to a first supply voltage level, and has its drain connected to a bias current source, and wherein a second one of said transistors has its source connected to a first supply voltage level, has its drain connected to the source of the input transistor, and has its gate connected to the gate and to the drain of the said first transistor; an output transistor, preferably a MOSFET, having its source connected to a first supply voltage level, and having its drain connected to the output terminal; current coupling means coupled between the drain of said input transistor and the gate of said output transistor;

wherein said current coupling means preferably comprise: two transistors, preferably MOSFETS, connected in current mirror configuration, wherein one transistor has its source connected to a second supply voltage level and has its drain connected to the drain of the input transistor, and wherein the other transistor has its source connected to said second supply voltage level, has its drain connected to a first bias current source and to the gate of said output transistor, and has its gate connected to the gate and to the drain of the said one transistor; an output current sensor associated with the output transistor, providing a sensor output current signal representing the output current; wherein the output current sensor preferably comprises a sensor transistor of the same conductivity type as the output transistor, having its source and gate connected in parallel to the source and gate of the output transistor; a current feedback loop feeding back a signal derived from the sensor output current signal to control said controllable impedance; wherein the current feedback loop preferably comprises: two transistors, preferably MOSFETS, connected in current mirror configuration, wherein one transistor has its drain connected to receive said sensor output current signal and wherein the other transistor has its drain connected to the source of the input transistor.

Appendix
Evidence (None)

Appendix
Related Proceedings (None)